Q.P. Code: 20CS0504 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations May-2022

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to CSE, CSIT, CSM & CIC)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Differentiate between I/O unit and memory Unit.	L4	4M
	b	Describe in detail about the Basic Operational Concepts with neat diagram.	L2	8M
		OR		
2	a	Discuss on basic I/O operations.	L2	6M
	b	Discuss about Bus structure with neat sketch.	L2	6M
		UNIT-II		
3	a	Illustrate the signed number representations.	L3	6M
	b	Explain fixed point representations.	L2	6M
		OR		
4	a	Prepare a flowchart for multiplication of positive numbers.	L6	4M
	b	Illustrate the steps multiplication algorithm with an example.	L3	8M
		UNIT-III		
5	a	Summarize the Register Representations and way it is used.	L5	6M
	b	Construct a 4-line common bus system with a neat diagram.	L6	6M
		OR		
6		Survey the Address Sequencing with neat diagram.	L4	12M
		UNIT-IV		
7	a	Assess the Memory Hierarchy with neat sketch.	L5	8M
	b	Differentiate between RAM & ROM.	L4	4M
		OR		
8	a	Compare various types of Auxiliary memory.	L2	6M
	b	Define track and sector. Analyze the importance of auxiliary memory.	L4	6M
		UNIT-V		
9	a	Construct 4-segment Instruction Pipeline and explain.	L6	6M
	b	Define the hazards? Explain in detail about instruction hazards.	L3	6M
		OR		
10		Categorize and discuss various forms of parallel processing based on Flynn's taxonomy with a neat sketch.	L4	12M

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